



IFR

\$

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE			
SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT		Docket Number: 2885/93	
Application Number 10/523,764	Filing Date August 2, 2005	Examiner K. McLean Mayo	Art Unit 2187
Invention Title DATA PROCESSING METHOD AND DEVICE		Inventors Martin Vorbach et al.	

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to:
Mail Stop: Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on
Date: August 22, 2007
Signature: *Michelle M. Carniaux* 59,210 for
Michelle M. Carniaux, Reg.No. 36, 098

Sir:

Pursuant to 37 CFR § 1.56, the attention of the Patent and Trademark Office is hereby directed to the reference(s) listed on the attached PTO-1449. Unless otherwise indicated herein, one copy of each reference is attached. It is respectfully requested that the information be expressly considered during the prosecution of this application, and that the reference(s) be made of record therein and appear among the "References Cited" on any patent to issue therefrom. The filing of this Information Disclosure Statement and the enclosed PTO Form No. 1449, shall not be construed as an admission that the information cited is prior art, or is considered to be material to patentability as defined in 37 C.F.R. § 1.56(b). The paragraphs marked below are applicable. It is believed that no fees other than those indicated below are due, but authorization is hereby given to charge any additional fees due, or to credit any overpayment, to Kenyon & Kenyon LLP, deposit account 11-0600.

☐ 1. This Information Disclosure Statement is being filed (a) within three months of the filing date of a national application other than a continued prosecution application under 37 C.F.R. §1.53(d), (b) within three months of the date of entry of the national stage as set forth in 37 C.F.R. § 1.491 in an international application, (c) before the mailing date of a first Office Action on the merits in the present application, OR (d) before the mailing of a first office action after filing of a request for continued examination. No certification or fee is required.

☒ 2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

☐ a. I hereby certify that each item of information contained in this Information Disclosure Statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(1).

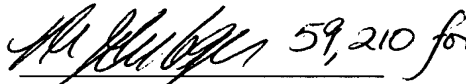
☐ b. I hereby certify that no item of information in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to my knowledge after making reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this Information Disclosure Statement. 37 CFR §1.97(e)(2).

☒ c. Please debit **Kenyon & Kenyon LLP, Deposit Account No. 11-0600** in the amount of **\$180.00** in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two copies of this paper are attached. 37 CFR §1.97(c)(2).

☒ 3. Since this application was filed after June 30, 2003, copies of U.S. references are not included.

Respectfully submitted,

Date: August 22, 2007


Michelle M. Carniaux
Reg. No. 36,098

KENYON & KENYON LLP
One Broadway
New York, NY 20004
(212) 425-200 telephone
(212) 425-5288 facsimile
CUSTOMER NUMBER 26646

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANTS
PTO-1449**

Attorney Docket No.
2885/93

Serial No.
10/523,764

Applicant(s)
Vorbach et al.

Filing Date
August 2, 2005

Group Art Unit
2187

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,233,667	November 11, 1980	Devine et al.			
	4,720,778	January, 1998	Hansen et al.			
	5,311,079	May 10, 1994	Ditlow et al.			
	5,392,437	February 21, 1995	Matter et al.			
	5,659,797	August 19, 1997	Zandveld et al.			
	5,737,516	April 1998	Circello et al.			
	5,841,973	November 1998	Cooke et al.			
	5,892,962	April 6, 1999	Cloutier			
	5,926,638	July 1999	Inoue			
	5,960,200	September 1999	Eager et al.			
	5,996,083	November 30, 1999	Gupta et al.			
	6,003,143	December 1999	Kim et al.			
	6,170,051	January 2001	Dowling,			
	6,211,697	April 2001	Lien et al.			
	6,212,650	April 2001	Guccione, Steven A.			
	6,282,701	August 2001	Wygodny et al.			
	6,286,134	September 2001	Click, Jr. et al.			
	6,301,706	October 2001	Maslennikov et al.			
	6,398,383	June 2002	Huang			
	6,421,917	July 16, 2002	Mohan			
	6,434,695	August 2002	Esfahani et al.			
	6,437,441	August 2002	Yamamoto			
	6,504,398	January 2003	Lien et al.			
	6,721,830	April 2004	Vorbach et al.			
	2003/0056085	March 2, 2003	Vorbach			
	2003/0123579	July 3, 2003	Safari et al.			
	2003/0192032	October 2003	Andrade et al.			
	2004/0199688	October 2004	Vorbach et al.			

FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	0 208 457	January 14, 1987	Europe				
	1 102 674	May 30, 2001	Europe				
	0 696 001	December 5, 2001	Europe				
	WO99/12111	March 11, 1999	PCT				
	WO01/55917	August 2, 2001	PCT				

INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449	Attorney Docket No. 2885/93	Serial No. 10/523,764
	Applicant(s) Vorbach et al.	
	Filing Date August 2, 2005	Group Art Unit 2187

						TRANSLATION	
	8-44581	February 16, 1996	Japan			Abstract	
	7-154242	June 16, 1995	Japan			Abstract	
	58-58672	April 7, 1983	Japan			Abstract	
	2-226423	September 10, 1990	Japan			Abstract	
	5-276007	October 22, 1993	Japan			Abstract	
	8-250685	September 27, 1996	Japan			Abstract	
	2-130023	May 18, 1990	Japan			Abstract	
	11-307725	November 5, 1999	Japan			Abstract & Partial Translation	
	2000-181566	June 30, 2000	Japan			Computer Translation	
	9-27745	January 28, 1997	Japan			Abstract	

OTHER DOCUMENTS

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Abnous, A., et al., "The Pleiades Architecture," Chapter I of <i>The Application of Programmable DSPs in Mobile Communications</i> , A. Gatherer and A. Auslander, Ed., Wiley, 2002, pp. 1-33.
	Chen et al., "A reconfigurable multiprocessor IC for rapid prototyping of algorithmic-specific high-speed DSP data paths," <i>IEEE Journal of Solid-State Circuits</i> , Vol. 27, No. 12, December 1992, pp.1895-1904.
	Hastie et al., "The implementation of hardware subroutines on field programmable gate arrays," Custom Integrated Circuits Conference, 1990, Proceedings of the IEEE 1990, May 16, 1990, pp. 31.3.1 – 31.4.3 (3 pages).
	Kastrup, B., "Automatic Hardware Synthesis for a Hybrid Reconfigurable CPU Featuring Philips CPLDs," Proceedings of the PACT Workshop on Reconfigurable Computing, 1998, pp. 5-10.
	Razdan et al., "A High-Performance Microarchitecture with Hardware-Programmable Functional Units, Micro-27, Proceedings of the 27 th Annual International Symposium on Microarchitecture, IEEE Computer Society and Association for Computing Machinery, November 30- December 2, 1994, pp. 172-180.
	Siemers et al., "The >S<puter: A Novel Micoarchitecture Mode for Execution inside Superscalar and VLIW Processors Using Reconfigurable Hardware," Australian Computer Science Communications, Volume 20, No. 4, Computer Architecture, Proceedings of the 3 rd Australian Computer Architecture Conference, Perth, John Morris, Ed., February 2-3, 1998, pp. 169-178.
	Skokan, Z.E., "Programmable logic machine (A programmable cell array)," <i>IEEE Journal of Solid-State Circuits</i> , Vol. SC-18, No. 5, October 1983, pp. 572-578.
	Yeung, A. et al., "A data-driven architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, <i>Proceedings VLSI Signal Processing Workshop</i> , IEEE Press, pp. 225-234, Napa, October 1992.
	Yeung, A. et al., "A reconfigurable data-driven multiprocessor architecture for rapid prototyping of high throughput DSP algorithms," Dept. of Electrical Engineering and Computer Sciences, Univ. of California, Berkeley, USA, pp. 169-178, <i>IEEE</i> 1993.

EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	